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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,625	02/19/2002	Atsushi Sakai	50006-138	9551

7590 08/16/2004

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EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	10/076,625	SAKAI ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 July 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed ~~amendment(s)~~ request for reconsideration will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed ~~amendment(s)~~ request for reconsideration a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: *1-24*.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: Applicant's arguments are not persuasive.

With regard to Applicant's arguments relative to the rejection of claim 1 under 35 USC 102(b), the central issue is the interpretation of the phrase "the data movements run off the predicted behavior" which is found in the Fujiwara reference. Applicant acknowledges that Fujiwara teaches changing from software cache control to hardware cache control when "the data movements run off the predicted behavior", however, Applicant asserts that the disputed phrase does not expressly or inherently teach a cache miss. Applicant sets forth two alternative interpretations of the disputed phrase in an attempt to show that one skilled in the art would not necessarily interpret the phrase to mean a cache miss. These alternative interpretations are an arithmetic overflow and a processor exception.

Examiner contends that these alternative interpretations conspicuously ignore the context of the phrase as it appears in the Fujiwara reference. Fujiwara teaches a dual software/hardware cache control, where the loading and replacing of cache lines are mainly controlled by software as determined at compile time (§ 3.1.3, lines 1-5 and 8-10). Fujiwara further teaches that the software cache is predictive, acting before a request is made by the processor core (§ 3.1.3, lines 12-13). Fujiwara then states that because all data transfer tasks cannot be perfectly scheduled at compile time, the hardware cache control mode is provided (§ 3.1.3, lines 26-30). Fujiwara teaches that the change from software to hardware control occurs when "the data movements run off the predicted behavior" (§ 3.1.3, lines 32-36). In context, the "predicted behavior" of Fujiwara can only mean the loading and replacing of cache lines by the software cache controller before a request is made by the processor. Therefore, the phrase "running off the predicted behavior" must mean that the data requested by the processor does not correspond to the data loaded into the cache by the software controller, or in other words, a cache miss occurs. This interpretation is further supported by Fujiwara's description of the events following the occurrence of data movements running off the predicted behavior: The cache is switched to hardware control where a write back occurs, and the hardware control causes a cold miss (§ 3.1.3, lines 36-39). Therefore, it is readily apparent that a miss under software control is propagated to the hardware control so that the appropriate cache line may be fetched, and that this is necessary because the predictive nature of the software cache control renders it incapable of responding to a miss resulting from an imperfect prediction.

Thus, it may be seen in context that the phrase "the data movements run off the predicted behavior" cannot mean an arithemetic overflow or processor exception, because by Applicant's own admission these events do not cause a cache miss to occur (see Applicant's remarks on page 4). Furthermore, Applicant has provided no explanation as to the significance of such alternative interpretations in the context of Fujiwara's teachings relative to a dual software/hardware cache control.

Examiner again emphasizes that inherency has not been relied upon in reaching these conclusions. Fujiwara has used the phrase "the data movements run off the predicted behavior" to have precisely the same meaning as a cache miss. This is the only reasonable interpretation of the phrase in the context of Fujiwara's teachings as illustrated above.

With regard to Applicant's arguments relative to the rejection of claim 2 under 35 USC 102(b), Examiner contends that the referenced portion of Fujiwara does indeed describe an automatic process (i.e. self-acting or self-regulating). The system described by Fujiwara detects a cache miss and causes a changeover from software to hardware cache control, thereby acting upon itself to regulate its own operation.

With regard to Applicant's arguments relative to the rejection of claims 3 and 4 under 35 USC 102(b), Examiner maintains that the referenced portion of Fujiwara teaches storing data in the cache in accordance with code produced by static prediction of a compiler. Fujiwara teaches a cache where loading and replacing of lines are controlled by software, where such management is carried out by a Data Transfer Controller that executes instructions generated at compile time.

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SPE, TC2100